30.4 40GHz Wide-Locking-Range Regenerative Frequency Divider and Low-Phase-Noise Balanced VCO in 0.18µm CMOS

Jun-Chau Chien, Liang-Hung Lu

National Taiwan University, Taipei, Taiwan

Frequency dividers and VCOs are the most critical building blocks for the implementation of high-frequency signal sources that are widely used in wireline and wireless communication systems. In this paper, circuit topologies are presented to improve the performance of these high-frequency components. For the frequency divider, the proposed g_m-enhancement technique incorporates the series and shunt inductive peaking in the resonator design. With the regenerative mechanism in the injection-locked frequency divider, a wide locking range can be achieved without using varactors for frequency tuning. As for the VCO, a balanced architecture is proposed for low phase noise while relaxing the stringent requirement on the start-up conditions at higher frequencies. Both of the circuits are designed and fabricated in a 0.18µm CMOS process.

Injection-locked frequency dividers loaded with on-chip resonators are used to provide high-speed frequency division at low power consumption [1]. However, the limited locking range due to the high-Q resonators makes it difficult to cover the frequency tuning range of the VCOs under process and temperature variations. Tuning the free-running frequency with the varactors at the cost of a more complicated controlled mechanism when the divider is integrated in a system can extend the operating range of the divider. Alternatively, a regenerative divider with inductive loads presents an enhanced input bandwidth [2]. Due to the use of the mixer in the regenerative loop, higher power consumption is typically required. To overcome the design limitations, a g_m-enhancement technique to increase the loop gain for regenerative frequency division is proposed. Figure 30.4.1 shows the block diagram of a regenerative divider that consists of a feedback loop with a mixer and a band-pass filter. As the input signal ω_{in} mixes with the feedback signal $\omega_{in}/2$, frequency components of $3\omega_{in}/2$ and $\omega_{in}/2$ are generated at the output of the mixer. With the selectivity of the LC-tank, frequency division is achieved provided that the open-loop gain for the component at $\omega_{in}/2$ exceeds unity. Consequently, it is desirable to maximize theloop-gain in the circuit design for wideband operations. A conventional circuit topology of the frequency divider is shown in Fig. 30.4.1, where the switching transistor M_1 acts as the mixer and the cross-coupled pair with the LC-tank forms the feedback loop [3]. As the RF signal applies at the gate, M_1 can be treated as a passive drain-pumped mixer [4]. By biasing the gate voltage higher than the threshold voltage, the transconductance of M_1 is a nonlinear function of the drain voltage V_{ds}. To maximize the effective transconductance $g_{m,eff}$ for an enhanced conversion gain, a series inductive peaking technique is adopted. By inserting the inductor L_s in series with M_1, the effective drain voltage $V_{ds,eff}$ increases as long as $\omega_s > \sqrt{[(\omega_{LO}^2+\omega_d^2)/2]}$, where $\omega_s=(L_sC_d)^{-1}$ and $\omega_d=(R_{ds}C_d)^{-1}$. Note that the maximum $V_{ds,eff}$ is obtained with $\omega_s=\sqrt{(\omega_{LO}^2+\omega_d^2)}$. Therefore, by choosing the value of L_s for the desirable resonant frequency ω_s, a significant increase in the $g_{m,eff}$ and the loop gain is achieved. Figure 30.4.2 shows the circuit schematic of the 40GHz regenerative frequency divider with the series-peaking technique. The inductor L_s is designed to resonate with the parasitic capacitance C_d at the frequency of 32GHz. The simulated voltage waveforms and input sensitivity curves are demonstrated in Fig. 30.4.2. It is obvious that the proposed circuit technique effectively increases the voltage amplitude at the drains of the switching transistor, leading to 2.5× improvement in the locking range of the frequency divider.

The cross-coupled LC-tank topology is widely used for the implementation of CMOS VCOs at millimeter-wave frequencies due to its low-power advantage. On the other hand, the balanced differential Colpitts oscillator features superior phase-noise property due to the cyclo-stationary noise effect [5]. However, such VCO requires higher loop gain for reliable oscillation start-up. Recently, VCOs combining the advantages of both techniques have been reported [5, 6], where the cross-coupled pair is stacked with the negative-resistance cell and an elevated supply voltage is required. An improved configuration, shown in Fig. 30.4.3, is proposed. With the capacitive feedback provided by the source resonator (L_s-C_s), which resonates at a frequency lower than the oscillation, the VCO exhibits low phase noise due to its resemblance to the Colpitts oscillators. In addition, the cross-coupled connection established by C_f and the feedback provided by L_g enhance the negative resistance [7], which in turn reduces the required bias current and minimizes the noise generation from the active devices. It is noted that due to the use of C_f in the cross-coupled connection, the gate of M_1 and M_2 can be biased at a current density for minimum noise figure through a current mirror. Based on circuit simulations, the required bias current of the proposed VCO for a sustained oscillation is reduced by 2× compared with conventional Colpitts oscillators.

The frequency divider and the VCO are fabricated in a standard 0.18µm CMOS process. On-wafer probing with the setup losses calibrated was employed to characterize the circuit performance. Experimental results of the divider are shown in Fig. 30.4.4. The regenerative divider, which self-oscillates at 23GHz, provides 2:1 frequency division for an input ranging from 37.5 to 49.8GHz. With an injected power level of -2dBm, the measured output power is -10±2dBm for the input frequency range from 38.6 to 49.2GHz and diminishes at the edge of the input locking range due to insufficient loop gain. When the divider is locked at an input frequency of 40GHz, the measured output spectrum and the respective phase noise are also characterized. Figure 30.4.5 shows the measurement results of the VCO including the output tuning characteristics, output spectrum, and close-in phase noise. The VCO exhibits a frequency tuning range from 39.2 to 40.3GHz (2.75%) and an output power of -8dBm with a variation less than ±0.9dB, while the measured phase noise at 1MHz offset is -108.65dBc/Hz. Both the frequency divider and VCO consume 6mA from a 1V supply excluding output buffers. Fig. 30.4.6 shows the performance summary and the comparison with prior arts. The micrographs of the fabricated circuits are shown in Fig. 30.4.7.

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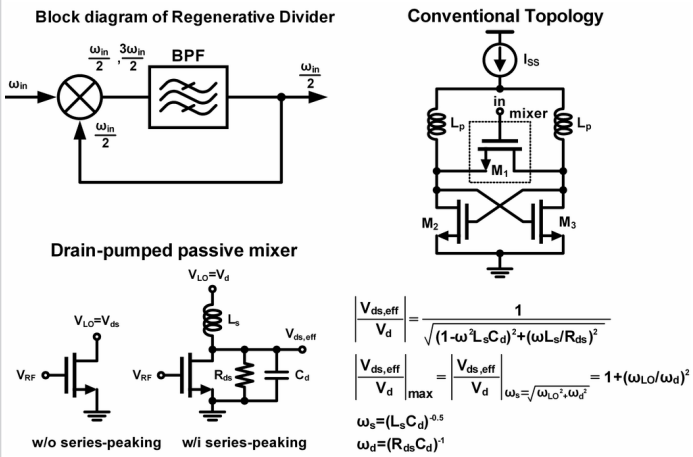

Figure 30.4.1: Block diagram of the regenerative frequency divider and the drain-pumped passive mixer with the series-peaking technique.

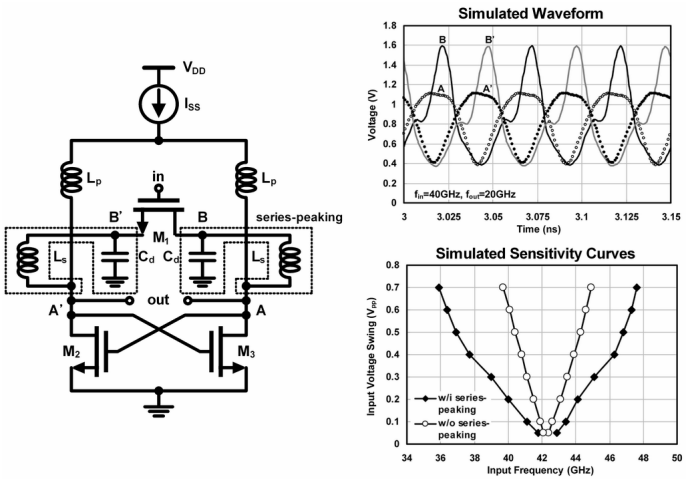

Figure 30.4.2: Circuit schematic of the proposed frequency divider and the simulation results.

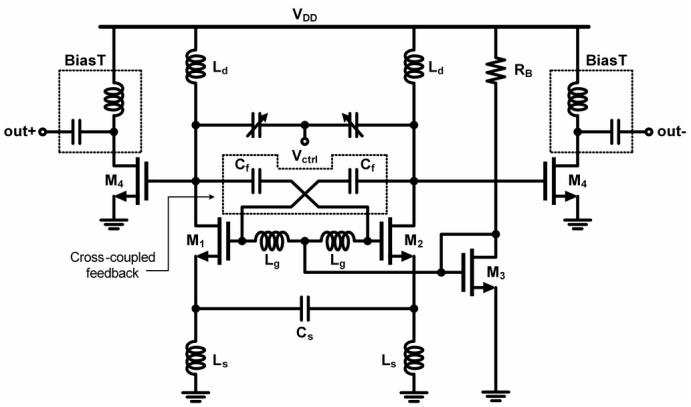

Figure 30.4.3: Circuit schematic of the proposed VCO circuit.

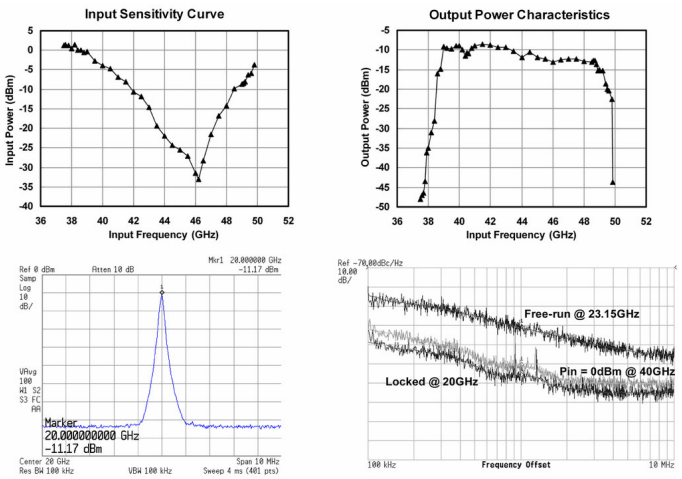

Figure 30.4.4: Measurement results of the 40GHz frequency divider.

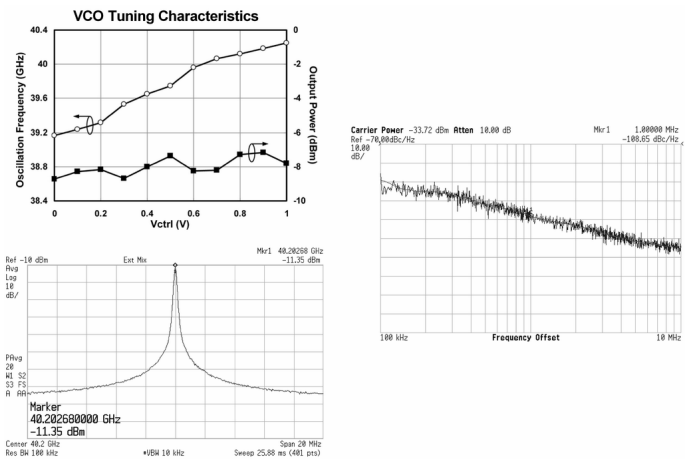

Figure 30.4.5: Measurement results of the 40GHz VCO.

Ref. Divider	Technology	Freq (GHz)	Pin (dBm)	Locking range (GHz)	VDD (V)	P_{diss} (mW)
This	0.18μm CMOS	40	0	10.6	1.0	6
H. Wu ISSCC01	0.35μm CMOS	19	5	1.35	1.2	1.2
J. Lee JSSC04	0.18μm CMOS	40	4	2.3	2.5	16.8
M. Tiebout JSSC04	0.13μm CMOS	40	15	1.5	1.5	3
K. Yamamoto ESSCIRC04	0.2μm CMOS	55	0	3.2	1.0	10.1
K. Yamamoto ISSCC06	90nm CMOS	70	0	8.7*	0.5	2.75

*varactors used

Ref. VCO	Technology	Freq (GHz)	FTR (%)	PN@1MHz (dBc/Hz)	VDD (V)	P_{diss} (mW)	FOM (dBc/Hz)
This	0.18μm CMOS	40	2.75	-108.6	1.0	6.0	-193
M. Tiebout ISSCC02	0.12μm CMOS	51	1.3	-85.0	1.5	1.5	-179
P.-C. Huang ISSCC05	0.13μm CMOS	114	2.1	-107.6*	1.2	8.4	-180
J. Kim ISSCC05	0.12μm SOI	44	9.8	-101	1.5	7.5	-185
J. Lee JSSC06	0.18μm CMOS	40	3.5	-90	1.3	1.0	-182
C. Cao JSSC06	0.13μm CMOS	59	9.8	-89	1.5	9.8	-175
D. Huang ISSCC06	90nm CMOS	60	0.16	-100	1.0	1.9	-193

FOM=PN+20log(f_o/Δf)-10log(P_{diss}/1mW) *at 10MHz offset

Figure 30.4.6: Performance summary and comparison table.

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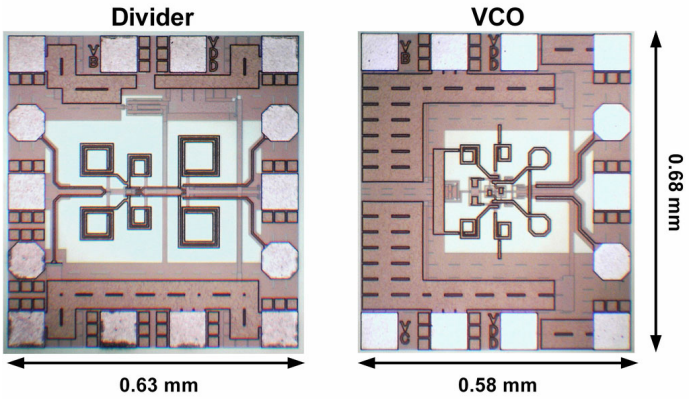

Figure 30.4.7: Micrographs of the fabricated circuits.

